



Serial No. 09/396,228

RCA 89141

10/7/03 #10
W. K. H. K.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant : K. Ramaswamy et al.

Serial No. : 09/396,228

Filed : September 15, 1999

For : OUTPUT SYMBOL RATE CONTROL IN A PACKET
TRANSPORT RATE CONVERSION SYSTEM

Examiner : Melanie Jagannathan

Art Unit : 2666

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BRIEF ON APPEAL

May It Please The Honorable Board:

Appellants appeal the final rejection of Claims 1-13 of the above-identified application in the Final Rejection dated April 7, 2003. The fee of \$320.00 for filing this Brief is to be charged to Deposit Account 07-0832.

Appellants waive an Oral hearing for this appeal.

Please charge any additional fee or credit any overpayment to the above-identified Deposit Account.

Three copies of the Brief are enclosed. This page is also submitted in duplicate for fee charging purposes.

I. REAL PARTY IN INTEREST

The real party in interest of Application Serial No. 09/396,228 is the assignee of record:

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II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-13, all the claims in the application after consideration of the response to the Final Rejection, are rejected.

Claims 1-13, all the rejected claims, are appealed.

IV. STATUS OF AMENDMENTS

All amendments were entered and are reflected in the claims included in Appendix I.

V. SUMMARY OF THE INVENTION

In accordance with the principles of the present invention defined by claim 1, a remodulator system apparatus controls the bit rate of an output packet stream. An input packet buffer, coupled to an input transport packet stream source, generates a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor

full. An output packet stream generator coupled to the input packet stream buffer responds to an output clock signal for generating the output packet stream in synchronism with the output clock signal. A variable output clock signal generator responds to a control signal that is generated in response to the status signal.

Independent method claim 8 contains limitations similar to those recited in claim 1.

VI. ISSUES

Whether the subject matter of Claims 1-2, 5-7, 8-9 is unpatentable under 35 U.S.C. 102(b) over Sato et al.

Whether the subject matter of Claims 3 and 10 is unpatentable under 35 U.S.C. 103(a) over Sato et al. in view of Sartain et al.

Whether the subject matter of Claim 4 is unpatentable under 35 U.S.C. 103(a) over Sato et al.

Whether the subject matter of Claim 12 is unpatentable under 35 U.S.C. 103(a) over Sato et al. in view of Horton.

Whether the subject matter of Claims 11 and 13 is unpatentable under 35 U.S.C. 103(a) over Sato et al. in view of Kostreski et al.

VII. GROUPING OF THE CLAIMS

Claims 1 – 7 stand together and Claims 8 – 13 stand together.

VIII. ARGUMENTS

Sato et al. do not anticipate the present claimed invention. Nor does the combination of Sato et al. with any of Sartain et al., Horton or Kostreski et al anticipate or render the present claimed invention unpatentable. Thus, withdrawal of the Final Rejection of Claims 1-2, 5-7, 8-9 under 35 U.S.C. 102(b) and Claims 3, 4 and 10 – 13 under 35 U.S.C 103(a) is respectfully requested.

Overview of the Cited References

Sato et al. discloses a method of transmitting timing-critical data, such as MPEG transport stream packets, via an asynchronous channel. The packets are processed serially through a remultiplexer to obtain a constant rate, and are delivered to and processed by one or more target decoders. To prevent overflow of the transport buffers inside these decoders, a single monitor-scheduler monitors the transport buffers and delivers to each buffer the packets to be scheduled, so as to avoid buffer overflow and loss of information. The method also includes restamping the transport packets with new PCRs.

Sartain et al. dynamically compensates for differences in data rates for multistreamed systems, wherein any or all of the streams in a multidimensional system may be individually compensated at one time. The status of an input buffer is monitored and used to change the number of oversamples within a frame of one of the number of streams. Alternatively, a high frequency system clock is used to stall one of the streams for one or more clock cycles. In both of the above described compensation methods, distortion due to differences in data rates is reduced.

Horton discloses a digital television system which processes television information in the form of a stream of data packets representing compressed video and audio information, such as MPEG. The system includes on-screen display (OSD) provisions for displaying sophisticated graphics, such as animation, by storing graphics

data in read-only memory (ROM) in the same form as that used for video information. The graphics data is transported to the same video decoding and decompression unit which processes video data contained in video packets to form digital signals representing video information in uncompressed form, where it is converted in the same manner as video data to form graphic image data. A multiplexing arrangement is provided so that digital signals representing static graphics can be multiplexed with digital signals representing static graphics image data derived from bit mapped representations.

Kostreski et al. discloses dynamic programming of a digital entertainment terminal so that the terminal offers a variety of functionally different broadband services. A network interface module couples the terminal to a specific type of communication network for receiving a digital broadband channel. A VIP program map that identifies the available video information service providers (VIPs) on the basis of the location of their corresponding software control signals is downloaded on a narrow signaling channel of the terminal. The software control signals are transmitted cyclically to enable access by a random terminal at any time. A program memory captures the VIP program map and at least a portion of the software control signals received over the digital broadband channel as software executable by the control processor during turn-on of the terminal. When a GUIDE button is pressed, the terminal displays the available information service providers in accordance with the VIP program map, thereby enabling the user to access the broadband services offered by the selected information service provider.

The Rejection of claims 1-2, 5-7 and 8-9 under 35 U.S.C. § 102(b)

Claims 1-2, 5-7 and 8-9 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,566,174 (Sato et al.). Applicant respectfully traverses this rejection.

Claim 1 recites in pertinent part:

... an input packet buffer, ... generating a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full;
an output packet stream generator.... generating the output packet stream in synchronism with the output clock signal,
a variable output clock signal generator, responsive to a control signal, and
a control signal generator, responsive to the status signal, and generating the control signal.

Claim 8 recites in pertinent part:

...generating a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full;
generating the output packet stream in synchronism with the output clock signal;
generating a variable output clock signal in response to a control signal; and
generating the control signal in response to the status signal.

By varying the output clock signal in response to the status of the input packet buffer, it is possible to minimize the likelihood of input packet buffer underflow or overflow. This is illustrated in Fig. 1 and discussed in detail on page 8, lines 19-25 and page 9, lines 6-11 of applicant's specification.

Sato et al. do not disclose a variable output clock signal generator, which varies the output clock signal in response to a control signal that is generated in response to the status signal from the input packet buffer as in the present claimed invention. In addition, Sato et al. does not disclose an input packet buffer which generates a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full, as is recited in Independent Claims 1 and 8.

Instead, Sato et al. disclose a local clock 39 (Figs. 6 and 7) which produces a fixed output clock signal. There is no illustration of the local clock 39 being variable or receiving a control signal in Figs. 6 or 7, nor any such disclosure in the corresponding portion of the written description. Also, the Examiner has equated buffer 42 in Sato et

al. with the input packet buffer recited in claims 1 and 8. However, the status signal produced by buffer 42 of Sato et al. indicates only that there is at least one packet in buffer 42 (col. 9, lines 45-46); i.e. it is either empty or not.

The Examiner also states that Sato et al. disclose the "scheduler 45 (Figure 7, element 45) [for] sending control signal indicating packet can be read out in response to status signal indicating at least one packet in buffer i.e. showing buffer is not empty and is not full but neither empty or full." However, the scheduler 45 of Sato et al. merely "checks whether outputting of the packet in the packet source 44 will overflow the transport buffer 87" (see column 6, lines 51 – 53 and column 9, lines 50 – 54). Sato et al. neither disclose nor suggest that the buffer produces a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full, as is recited in claims 1 and 8. Thus, contrary to the assertions of the Examiner, the scheduler 45 of Sato et al. does not correspond to, nor function as the input packet buffer of the present claimed invention.

Claims 2 and 5-7, dependent from and further defining the invention recited in claim 1, and claim 9, dependent from and further defining the invention recited in claim 8, are deemed allowable over Sato et al. for the reasons given above with respect to claims 1 and 8. However, Applicant offers the following additional comments on the indicated subclaims.

Claim 2 recites in pertinent part:

... circuitry to generate the control signal to condition the variable output clock signal generator to increase its frequency if the status signal indicates that the input packet buffer is full, and decrease its frequency if the status signal indicates that the input packet buffer is empty.

Claim 9 recites in pertinent part:

... the variable output clock signal increases in frequency if the status signal indicates that the input packet

buffer is full, and decreases in frequency if the status signal indicates that the input packet buffer is empty.

Because Sato et al. does not disclose a variable output clock signal generator, and because Sato et al. does not disclose an input packet buffer generating a status signal indicating whether the input packet buffer is full, empty or neither full or empty, as is recited in claims 1 and 8, it cannot include a control signal generator which generates a control signal to condition the variable output clock signal generator to increase its frequency if the status signal indicates that the input packet buffer is full, and decrease its frequency if the status signal indicates that the input packet buffer is empty, as is recited in claims 2 and 9.

Accordingly, it is respectfully submitted that claims 1-2, 5-7 and 8-9 are not anticipated by Sato.

The Rejection of claims 3 and 10 under 35 U.S.C. 103(a)

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1598 (Fed.Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (CCPA 1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion, or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. *Uniroya, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed.Cir. 1988), *cert. denied*, 488 U.S. 825 (1988); *Ashland Oil Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 28, 293, 227 USPQ 657, 664 (Fed.Cir. 1985), *cert. denied*, 475 U.S. 1017 (1986); *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed.Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a *prima facie* case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed.Cir. 1992).

The Examiner has rejected claims 3 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Sato et al. in view of Sartain et al U.S. Patent 6,169,747. Applicant respectfully traverses this rejection and points out that for a combination of art to render a claim unpatentable, that combination must disclose or suggest each and every limitation of the claim.

Claim 3 depends from claim 2, which in turn depends from independent claim 1. Claim 10 depends from claim 9, which in turn is dependent from independent claim 8.

Claim 3 recites in pertinent part:

... the input packet buffer generates the status signal further indicating whether the input packet buffer is: nearly full, or nearly empty;

the control signal generator further comprises circuitry to generate the control signal to condition the variable output clock signal generator to increase its frequency if the status signal indicates that the input packet buffer is nearly full, and decrease its frequency if the status signal indicates that the input packet buffer is nearly empty.

Claim 10 recites in pertinent part:

the status signal further indicates whether the input packet buffer is: nearly full, or nearly empty; and

the control signal conditions the variable output clock signal to increase its frequency if the status signal indicates that the input packet buffer is nearly full, and decrease its frequency if the status signal indicates that the input packet buffer is nearly empty.

As discussed in detail above, Sato et al. do not disclose or suggest a variable output clock signal generator nor a control signal generator for controlling the variable output clock signal generator in response to the status of the input packet buffer, nor an input packet buffer generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claims 1 and 8. Sato et al.

further do not disclose or suggest an input packet buffer generating a status signal further indicating whether the input packet buffer is nearly full or nearly empty, as is recited in claims 2 and 9.

Because Sato et al. do not disclose or suggest generating a status signal indicating whether the input packet buffer is empty, nearly empty, nearly full, full or neither full nor empty, Sato et al. cannot disclose generating a control signal so that the variable output clock signal generator increases its frequency if the status signal indicates that the input packet buffer is full or nearly full and decreases its frequency if the status signal indicates that the input packet buffer is empty or nearly empty, as is recited in claims 2, 3, 9 and 10.

Sartain et al. also do not disclose a variable output clock signal generator nor a control signal generator for controlling the variable output clock signal generator in response to the status of the input packet buffer, as is recited in claims 1 and 8. Further, Sartain et al. do not disclose generating the control signal so that the variable output clock signal generator increases its frequency if a status signal from an input packet buffer indicates that the input packet buffer is full or nearly full and decreases its frequency if the status signal indicates that the input packet buffer is empty or nearly empty, as is recited in claims 2, 3, 9 and 10.

Instead, Sartain et al disclose an oversampled digital-to-analog converter (DAC) system. An input buffer 111 holds input digital samples and generates a status signal indicating underflow, overflow, near underflow and near overflow conditions. Because a DAC generates an analog signal having a level corresponding to the values of successive input samples, there cannot be a source of an input packet stream, nor an input packet buffer. Also because a DAC system generates an analog output signal, there cannot be an output packet stream generator generating the output packet stream in synchronism with an output clock signal, nor a variable output clock signal generator, nor a control signal generator controlling the output clock signal generator, as recited in claims 1 and 8.

More specifically, Sartain discloses a sample input buffer 111 which generates a status signal indicating whether it is full (overflow) or empty (underflow) or nearly full (near overflow) or nearly empty (near underflow) as in the present claimed invention. An interpolation filter interpolates a number (e.g. 128 in Sartain) of oversamples in a frame between each input sample received from the input buffer 111. In order to minimize overflow and/or underflow of downstream circuitry, the interpolation filter is controlled in response to the status of the input buffer 111 to vary the number of interpolated oversamples in a frame. In one embodiment (Fig. 6), the coefficients of a variable interpolation filter 145 are varied to change the number of oversamples in a frame (col. 4, lines 28-35). That is, depending on the state of the input buffer 111, either more (e.g. 129) or fewer (e.g. 127) oversamples are produced in a frame (col. 4, lines 60-66). In another embodiment (Fig. 7), a fixed number (e.g. 128) of oversamples are produced by the interpolation filter 143 but some oversamples are either repeated or dropped (col. 5, lines 12-19). In yet another embodiment (Fig. 8) a fixed number of oversamples (e.g. 128) are produced by the interpolation filter 149, but a master clock 151 is stalled for one or more clock cycles depending on the status of the input buffer 111 (col. 5, lines 62-67). There is no disclosure or suggestion of an output packet stream generator responsive to a variable output clock signal generator whose frequency changes based on the of the input packet buffer being full or nearly full, or empty or nearly empty, as is recited in applicant's claims 3 or 10 of the present invention.

The references cited by the Examiner, taken singly or in combination, neither disclose or suggest an output packet stream generator responsive to a variable output clock signal generator generating an output clock signal conditioned to increase frequency when the status signal indicates that the input packet buffer is full, or nearly full, and to decrease frequency when the status signal indicates that the input packet buffer is empty or nearly empty, as is recited in claims 3 and 10.

In view of the above remarks, it is respectfully submitted that Sato et al. adds nothing when taken alone or in combination with Sartain et al that would make the present invention unpatentable.

The Rejection of claim 4 under 35 U.S.C. 103(a)

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Sato et al. Applicant respectfully traverses this rejection and points out that to support a 35 U.S.C. § 103(a) rejection, the reference must provide the motivation to be modified in the manner suggested by the Examiner.

Claim 4 recites in pertinent part, "... if the status signal indicates that the input packet buffer is full, null packets are deleted from the input transport packet buffer." As discussed in detail above, Sato et al. do not disclose or suggest a variable output clock signal generator nor a control signal generator for controlling the variable output clock signal generator in response to the status of the input packet buffer, nor an input packet buffer generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 1. Sato et al. also do not disclose or suggest deleting null packets from the input transport packet buffer if the status signal indicates that the input packet buffer is full, as is recited in claim 4 of the present invention.

Instead, in Fig. 3 of Sato et al., Sato et al. discloses circuitry 82 for unconditionally removing any null packet from the input packet stream (col. 5, lines 30-31). Furthermore, buffer 42, specified by the Examiner as corresponding to the input packet buffer recited in claim 1, does not provide a status signal indicating that it is full. Instead, the status signal from buffer 42 indicates only that there is at least one packet in the buffer 42, i.e. whether the buffer is empty or not (col. 9, lines 45-46). Because Sato et al. already disclose circuitry for handling null packets in the input packet stream, there is no motivation to modify Sato et al. in the extensive manner suggested by the Examiner to handle null packets in a the manner recited in claim 4.

Applicant therefore submits that there is nothing in Sato et al. which would lead one skilled in the art to make the modifications suggested by the Examiner. Instead, it is submitted that the Examiner was led to suggest the modifications to Sato et al. only

with the benefit of Applicant's disclosure. This is impermissible hindsight. Further, as described above, Sato et al. does not disclose or suggest a variable output clock signal generator nor a control signal generator for controlling the variable output clock signal generator in response to the status of the input packet buffer, nor an input packet buffer generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 1 of the present invention. Sato et al. also do not disclose or suggest deleting null packets from the input transport packet buffer if the status signal indicates that the input packet buffer is full, as is recited in claim 4 of the present invention.

The Rejection of claim 12 under 35 U.S.C. 103(a)

Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Sato et al. in view of Horton (U.S. Patent 5,969,770). Applicant respectfully disagrees.

Claim 12 depends from independent claim 8, and recites in pertinent part, "...the source of input transport packet stream represents auxiliary on-screen display (OSD) information."

As discussed in detail above, Sato et al. do not disclose or suggest generating a variable output clock signal responsive to a control signal, nor generating a control signal in response to the status signal from an input packet buffer, nor generating an input packet buffer status signal indicating whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 8. Referring to Fig. 3, while Sato et al. disclose a source 16 of auxiliary packets to be multiplexed into the packet stream to be recorded, that auxiliary packet source does not carry data representing on-screen display information, as is recited in applicant's claim 12. Instead, these auxiliary packets are termed "trickmode" packets in Sato et al. There is no detailed description in Sato et al. of what trickmode packets are, but it is stated that trickmode packets "can be generated from the incoming transport stream." This does not suggest the use of trickmode packets for on-screen display information, which are generally independent

of the incoming transport packet stream and usually predetermined fixed images which are stored in a read-only memory (ROM).

Horton does not disclose or suggest generating an output packet stream in synchronization with the output clock signal as is recited in claim 8. Therefore Horton cannot disclose or suggest generating a variable output clock signal in response to a control signal, nor generating a control signal in response to the status of the input packet buffer, nor generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 8.

Instead, Horton discloses a receiver for receiving a transport packet stream (1507) and processing the packet stream to produce the sound (21a, 21b) and image (19) of the selected television program, including selected on-screen display images produced from MPEG graphics information (1525-5) previously stored in the ROM 1525. Input packets are received and stored in an input packet buffer 1513, the data in the packets is then extracted and used to produce the sound and image of the television program. MPEG packets representing an on-screen display are stored in ROM 1525 and are processed in the transport processor 1507, as appropriate, to generate the on-screen display. There is no output packet stream as in the present claimed invention.

Neither Sato et al. nor Horton disclose or suggest generating a variable output clock signal nor generating a control signal for controlling the variable output clock signal in response to the status of the input packet buffer, nor generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 8.

The Rejection of claims 11 and 13 under 35 U.S.C. 103(a)

Claims 11 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sato et al in view of Kostreski et al. (U.S. Patent 5,734,589). Applicant disagrees.

Claim 11 depends from independent claim 8, and recites in pertinent part, "... the input packet stream format is compatible with one of a QAM or QPSK modulation format; and the output packet stream format is compatible with an 8-VSB or 16-VSB modulation format."

Claim 13 depends from independent claim 8, and recites in pertinent part, "... the input packet stream format is compatible with one of QAM, QPSK or VSB modulation formats; and the output packet stream format is compatible with a different one of said QAM, QPSK or VSB modulation formats."

As discussed in detail above, Sato et al. do not disclose or suggest generating a variable output clock signal responsive to a control signal, nor generating a control signal in response to the status signal from an input packet buffer, nor generating an input packet buffer status signal indicating whether the input packet buffer is full, empty, or neither empty nor full, as recited in claim 8.

Kostreski et al. also do not disclose or suggest generating a status signal indicating whether an input packet buffer is full, empty or neither empty nor full, nor generating a variable output clock signal in response to a control signal, nor generating the control signal in response to the status signal, as is recited in claim 8.

Instead, Kostreski et al. discloses a television and digital signal (audio, video, data) distribution system. The essence of Kostreski et al. is that set top boxes at consumer locations include a processor which can receive programs and data dynamically via one or more channels transmitted through the distribution system. In Fig. 3 of Kostreski, analog television signals are received in analog AM-VSB form (316), digital television signals are received in MPEG format (318), and other digital signals are received in ATM packets (401), possibly modulated in any one of several disclosed formats: QPSK, QAM, VSB, etc. The television and digital signals are converted to RF channels and combined (315), and then supplied (303) to a distribution network (309, 311) in any one of several disclosed formats, which may be different from the format in which the data was received.

Although the presence of input packet buffers in Kostreski et al. may be implied by the illustrated packet processing, there is no disclosure of any method for controlling the timing of the processing of those packets, and in particular no disclosure or suggestion of generating a variable output clock signal. More specifically, there is no disclosure or suggestion of generating a variable output clock signal responsive to a control signal, nor generating a control signal in response to the status signal from an input packet buffer, nor generating an input packet buffer status signal indicating whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 8.

In view of the above remarks, it is respectfully submitted that Sato et al. adds nothing when taken alone or in combination with Kostreski et al. that would make the present claimed invention unpatentable.

IX. CONCLUSION

For the reasons given above, it is respectfully submitted that the claims of the application satisfy the requirements of 35 U.S.C. § 102 and 35 U.S.C. §103, and removal of the rejections of claims 1-13 is respectfully requested.

Respectfully submitted,

K. Ramaswamy et al

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CERTIFICATE OF MAILING

I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to the Commissioner for Patents Alexandria, VA 22313 on:

September 18, 2003
Date

Linda Tindall
Linda Tindall

APPENDIX I

APPEALED CLAIMS

1. In a remodulator system, apparatus for controlling the bit rate of an output packet stream, comprising:
 - a source of an input transport packet stream;
 - an input packet buffer, coupled to the input transport packet stream source, for generating a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full;
 - an output packet stream generator, coupled to the input packet stream buffer, and responsive to an output clock signal, for generating the output packet stream in synchronism with the output clock signal,
 - a variable output clock signal generator, responsive to a control signal; and
 - a control signal generator, responsive to the status signal, and generating the control signal.
2. The system of claim 1 wherein:
 - the variable output clock signal generator is responsive to the control signal for varying the frequency of the output clock signal; and
 - the control signal generator comprises circuitry to generate the control signal to condition the variable output clock signal generator to increase its frequency if the status signal indicates that the input packet buffer is full, and decrease its frequency if the status signal indicates that the input packet buffer is empty.
3. The system of claim 2 wherein:
 - the input packet buffer generates the status signal further indicating whether the input packet buffer is: nearly full, or nearly empty;
 - the control signal generator further comprises circuitry to generate the control signal to condition the variable output clock signal generator to increase its frequency if the status signal indicates that the input packet buffer is nearly full, and decrease its frequency if the status signal indicates that the input packet buffer is nearly empty.

4. The system of claim 1 wherein:
the input transport packet stream contains null packets; and
if the status signal indicates that the input packet buffer is full, null packets are deleted from the input transport packet buffer.

5. The system of claim 1 further comprising:
a source of additional packets; wherein:
the output packet stream generator comprises a multiplexer, coupled to the input transport packet stream source and the additional packet source, for combining packets from the input transport packet stream and additional packets to generate the output packet stream.

6. The system of claim 5 wherein if the status signal indicates that the input packet buffer is empty, an additional packet is inserted into the output packet stream.

7. The system of claim 5 wherein the source of additional packets comprises:
a source of packets representing auxiliary data; and
a source of null packets; and
the multiplexer inserts an auxiliary data packet into the output packet stream as an additional packet if an auxiliary data packet is available, and inserts a null packet into the output packet stream as an additional packet if an auxiliary data packet is not available.

8. In a remodulator system, a method for controlling the bit rate of an output packet stream, comprising the steps of:
providing a source of an input transport packet stream;
storing input packet from said source in an input packet buffer;
generating a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full;

generating the output packet stream in synchronism with the output clock signal;

generating a variable output clock signal in response to a control signal; and
generating the control signal in response to the status signal.

9. The method of claim 8 wherein:

the frequency of the output clock signal varies in response to the control signal,
and

the variable output clock signal increases in frequency if the status signal indicates that the input packet buffer is full, and decreases in frequency if the status signal indicates that the input packet buffer is empty.

10. The method of claim 9 wherein:

the status signal further indicates whether the input packet buffer is: nearly full,
or nearly empty; and

the control signal conditions the variable output clock signal to increase its frequency if the status signal indicates that the input packet buffer is nearly full, and decrease its frequency if the status signal indicates that the input packet buffer is nearly empty.

11. The method of claim 8, wherein:

the input packet stream format is compatible with one of a QAM or QPSK modulation format; and

the output packet stream format is compatible with an 8-VSB or 16-VSB modulation format.

12. The method of claim 8, wherein:

the source of input transport packet stream represents auxiliary on-screen display (OSD) information.

13. The method of claim 8, wherein:
 - the input packet stream format is compatible with one of QAM, QPSK or VSB modulation formats; and
 - the output packet stream format is compatible with a different one of said QAM, QPSK or VSB modulation formats.

APPENDIX IITABLE OF CASES

1. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1598 (Fed.Cir. 1988).
2. *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (CCPA 1966).
3. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed.Cir. 1988), *cert. denied*, 488 U.S. 825 (1988).
4. *Ashland Oil Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 28, 293, 227 USPQ 657, 664 (Fed.Cir. 1985), *cert. denied*, 475 U.S. 1017 (1986).
5. *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed.Cir. 1984).
6. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed.Cir. 1992).

APPENDIX IIILIST OF REFERENCES

<u>U.S. Patent No.</u>	<u>Issue Date</u>	<u>Inventors</u>
5,566,174	October 15, 1996	Sato et al.
6,169,747 B1	January 2, 2001	Sartain et al.
5,969,770	October 19, 1999	Horton
5,734,589	March 31, 1998	Kostreski et al.

BRIEF ON APPEALTABLE OF CONTENTS

<u>ITEMS</u>	<u>PAGE</u>
I. Real Party of Interest	2
II. Related Appeals and Interferences	2
III. Status of Claims	2
IV. Status of Amendments	2
V. Summary of the Invention	2-3
VI. Issues	3
VII. Grouping of the Claims	3
VIII. Arguments	4-17
IX. Conclusion	17

APPENDIX

I. Appealed Claims	18-22
II. Table of Cases	23
III. List of References	23